Features

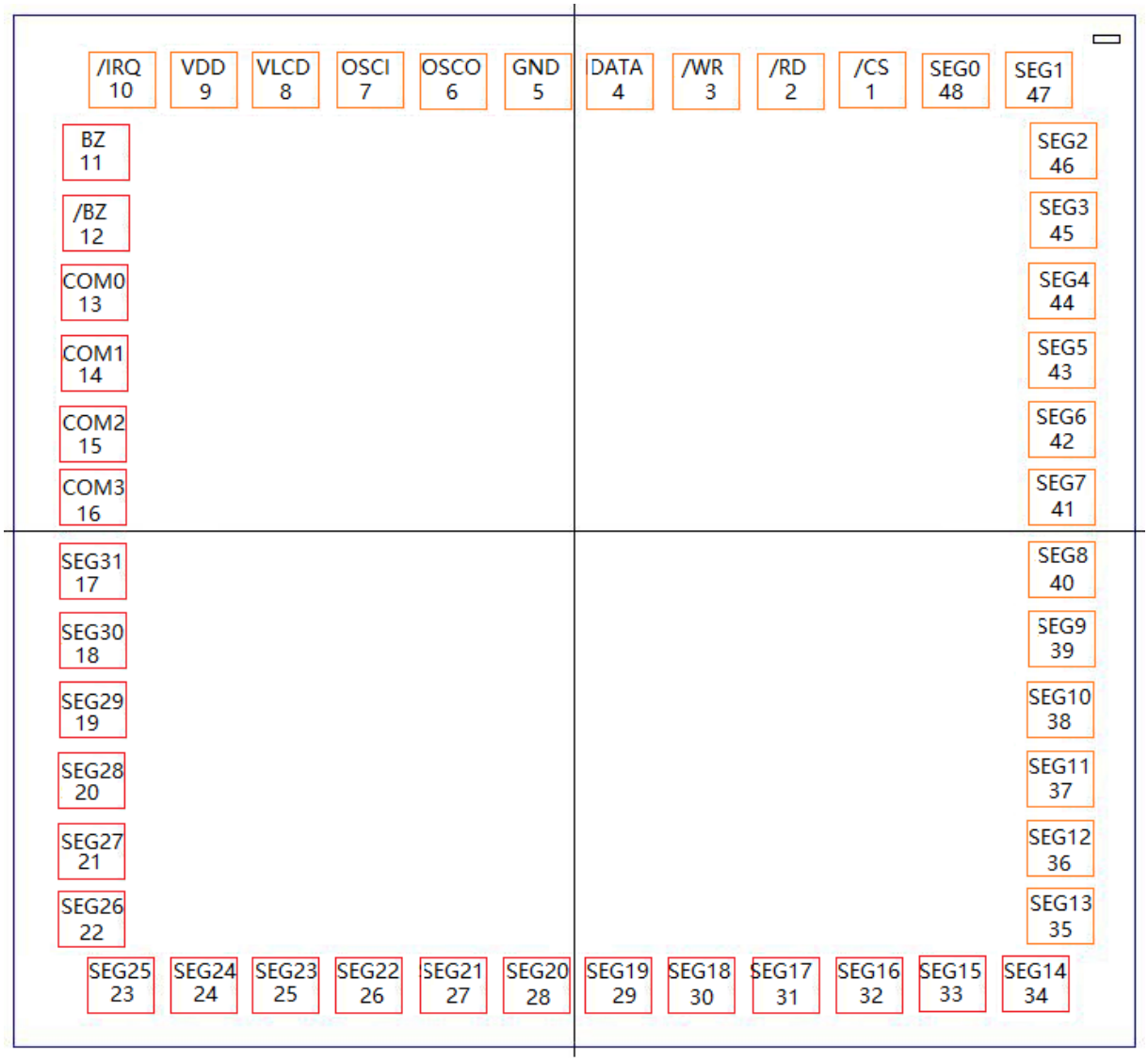
- Operating voltage:2.4-5.2V
- Built-in 256kHz RC oscillator（default）
- External 32.768kHz crystal（OSCO,OSCI）
- External 256kHz requency source（OSCI）
- Selection of 1/2 or 1/3 bias
- Selection of 1/2 or 1/3 or 1/4 duty
- Built-in 32×4 bit display RAM
- Selection of buzzer frequencies 2kHz、4kHz
- STANDBY mode（by Cmd LCD OFF,SYS DIS）
- 8 kinds of time base/WDT clock sources
- Time base or WDT overflow output （/IRQ pin）
- 3 or 4 wire serial interface
- Software configuration LCD parameters
- Data mode and command mode instructions
- Read/Write address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage（≤VDD）
- Package:
  SSOP48(300mil)(15.9mm x 7.5mm PP=0.635mm)
  LQFP48(7.0mm x 7.0mm PP=0.5mm)
  LQFP44(10.0mm x 10.0mm PP=0.8mm)
  SDIP28(288mil)(35.3mm x 7.3mm PP=2.54mm)
  DICE
  COG

1 General Description

VK1621 is a RAM Mapping 32x4 LCD Driver， It can support LCD screens with a maximum of 128 pattern(32SEGx4COM), it is also supports LCD screens of 2COM or 3COM.Only 3 or 4 lines are required to communication interface with the VK1621,it is used to configure display parameters and transfer display data, and can also enter the standby mode through Power down command.

2 COB PAD description and Coordinates

2.1 COBPAD Assignment



Chip size：1630×1755 um2　　Substrate：connected to VDD

PAD size：90×90 um　　PAD spacing：112 um

note：VLCD≤VDD

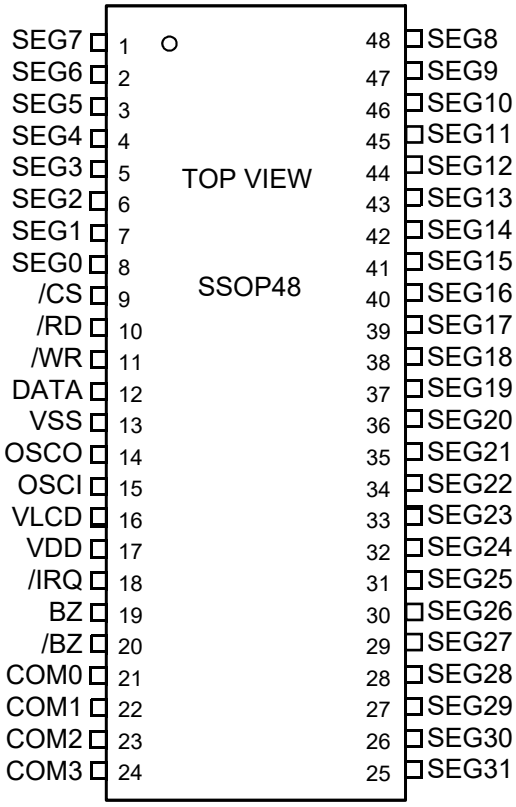
2.2 COB PAD Coordinates

coordinate origin is in the center of the chip, unit: μm

Pad No	Name	X	Y	Pad No	Name	X	Y
1	/CS	411.5	732.9	25	SEG23	-397.5	-738
2	/RD	298.5	732.9	26	SEG22	-282.5	-738
3	/WR	185.5	732.9	27	SEG21	-167.5	-738
4	DATA	63	732.9	28	SEG20	-52.5	-738
5	GND	-52	732.9	29	SEG19	62.5	-738
6	OSCO	-167	732.9	30	SEG18	177.5	-738
7	OSCI	-282	732.9	31	SEG17	292.5	-738
8	VLCD	-397	732.9	32	SEG16	407.5	-738
9	VDD	-512	732.9	33	SEG15	522.5	-738
10	/IRQ	-627.	732.9	34	SEG14	637.5	-738
11	BZ	-664.5	619.8	35	SEG13	675.5	-626
12	/BZ	-664.5	494	36	SEG12	675.5	-513
13	COM0	-664.5	382	37	SEG11	675.5	-400
14	COM1	-664.5	270	38	SEG10	675.5	-287
15	COM2	-664.5	158	39	SEG9	675.5	-174
16	COM3	-664.5	46	40	SEG8	675.5	-61
17	SEG31	-664.5	-66	41	SEG7	675.5	52
18	SEG30	-664.5	-178	42	SEG6	675.5	165
19	SEG29	-664.5	-290	43	SEG5	675.5	278
20	SEG28	-664.5	-402	44	SEG4	675.5	391
21	SEG27	-664.5	-514	45	SEG3	675.5	504
22	SEG26	-664.5	-626	46	SEG2	675.5	617
23	SEG25	-627	-738	47	SEG1	637.5	732.9
24	SEG24	-512.5	-738	48	SEG0	524.5	732.9

3 Pinouts and pin description

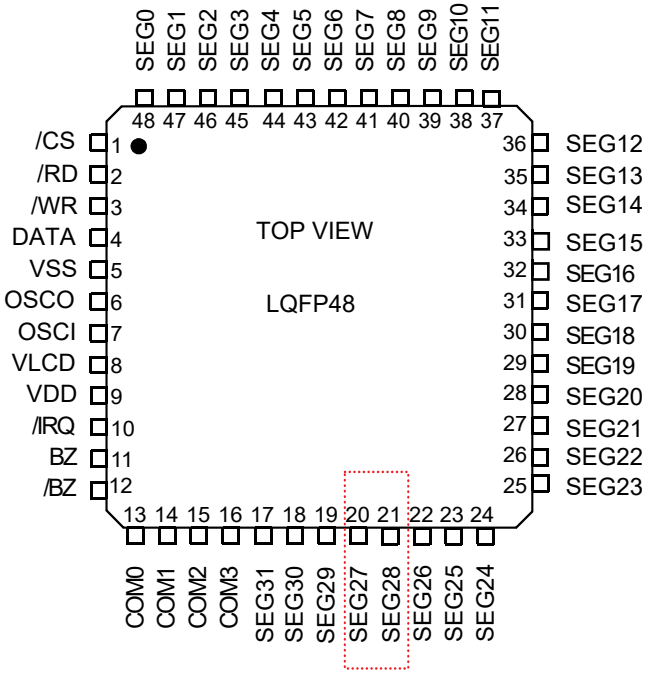
3.1 VK1621B SSOP48 Pin Assignment



3.2 VK1621B SSOP48 Pin Description

No.	Name	I/O	Function
1-8	SEG7-SEG0	O	LCD SEG outputs
9	/CS	I	Chip selection input with pull-up resistor 1-disabe，0-enable.
10	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.
11	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
12	DATA	I/O	Serial data input/output with pull-high resistor.
13	VSS	VSS	Negative power supply
14	OSCO	O	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
15	OSCI	I	
16	VLCD	I	LCD power input
17	VDD	VDD	Positive power supply
18	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
19	BZ	O	2kHz or 4kHz tone frequency output pair， when TONE OFF the BZ and /BZ pins output low level.
20	/BZ	O	
21-24	COM0-COM3	O	LCD COM outputs
25-48	SEG31-SEG8	O	LCD SEG outputs

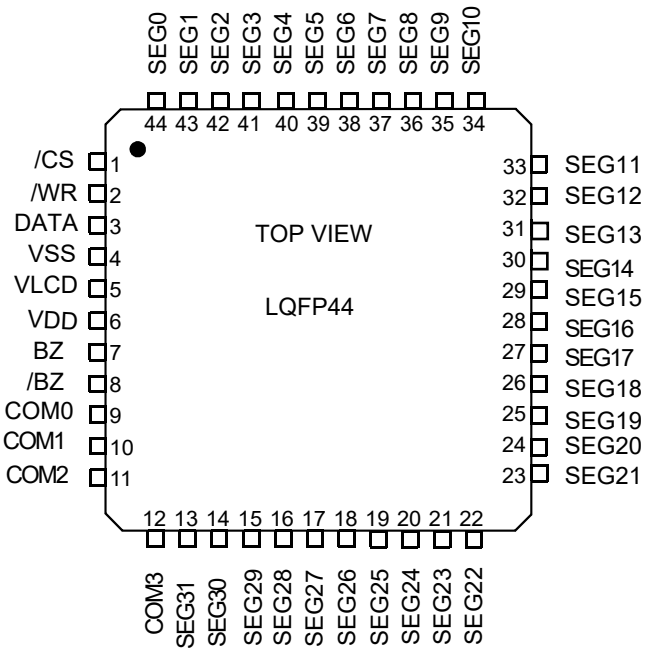
3.3 VK1621B LQFP48 Pin Assignment



3.4 VK1621B LQFP48 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip selection input with pull-up resistor 1-disabe，0-enable.
2	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data input/output with pull-high resistor.
5	VSS	VSS	Negative power supply
6	OSCO	O	Crystal oscillator: OSCI and OSCO pins are connected to a 32.768kHz crystal External clock source: OSCI pin is connected to a, external clock source On-chip RC oscillator: the OSCI and OSCO pins can be left open.
7	OSCI	I	
8	VLCD	I	LCD power input
9	VDD	VDD	Positive power supply
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output pair， when TONE OFF the BZ and /BZ pins output low level.
12	/BZ	O	
13-16	COM0-COM3	O	LCD COM outputs
17-19 22-48	SEG31-SEG29 SEG26-SEG0	O	LCD SEG outputs
20,21	SEG27,SEG28	O	LCD SEG outputs

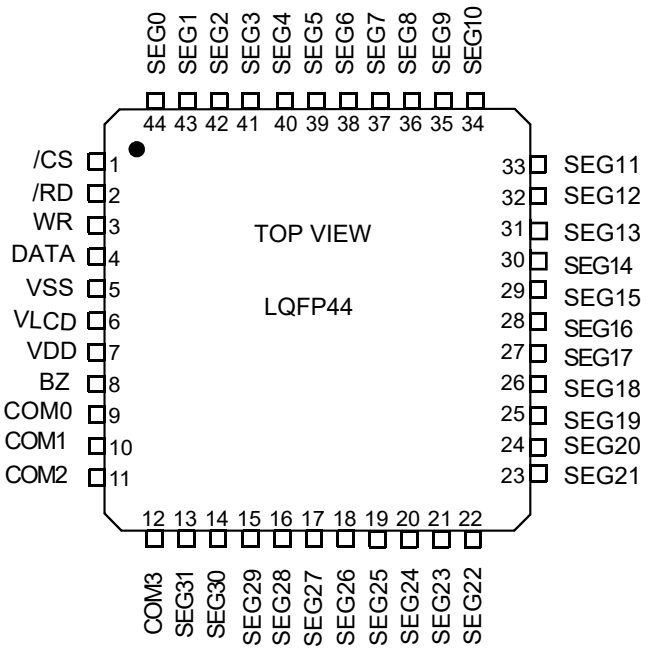
3.5 VK1621B LQFP44 Pin Assignment



3.6 VK1621B LQFP44 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip selection input with pull-up resistor 1-disabe，0-enable.
2	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
3	DATA	I/O	Serial data input/output with pull-high resistor.
4	VSS	VSS	Negative power supply
5	VLCD	I	LCD power input
6	VDD	VDD	Positive power supply
7	BZ	O	2kHz or 4kHz tone frequency output pair， when TONE OFF the BZ and /BZ pins output low level.
8	/BZ	O	
9-12	COM0-COM3	O	LCD COM outputs
13-44	SEG31-SEG0	O	LCD SEG outputs

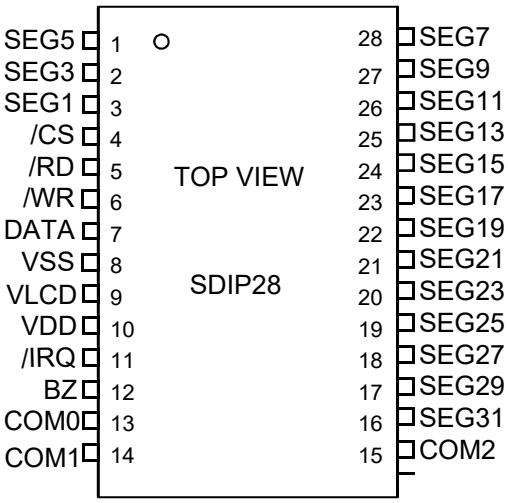
3.7 VK1621A LQFP44 Pin Assignment



3.8 VK1621A LQFP44 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip selection input with pull-up resistor 1-disabe，0-enable.
2	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data input/output with pull-high resistor.
5	VSS	VSS	Negative power supply
6	VLCD	I	LCD power input
7	VDD	VDD	Positive power supply
8	/BZ	O	2kHz or 4kHz tone frequency output， when TONE OFF the /BZ pin output low level.
9-12	COM0-COM3	O	LCD COM outputs
13-44	SEG31-SEG0	O	LCD SEG outputs

3.9 VK1621D SDIP28 Pin Assignment

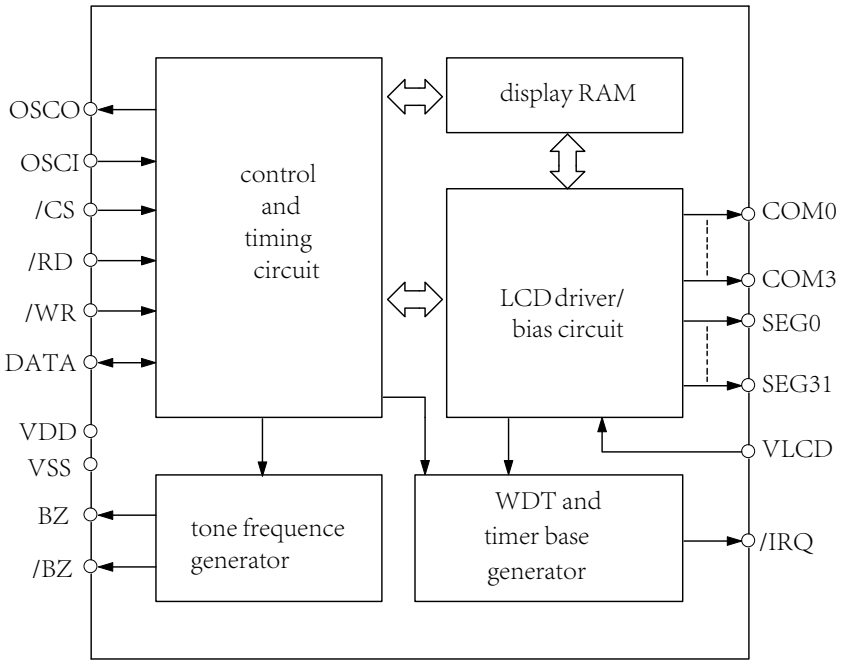


3.10 VK1621D SDIP28 Pin Description

No.	Name	I/O	Function
1,2,3	SEG1,3,5	O	LCD SEG outputs
4	/CS	I	Chip selection input with pull-up resistor 1-disabe，0-enable.
5	/RD	O	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.
6	/WR	O	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
7	DATA	I/O	Serial data input/output with pull-high resistor.
8	VSS	VSS	Negative power supply
9	VLCD	I	LCD power input
10	VDD	VDD	Positive power supply
11	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
12	BZ	O	2kHz or 4kHz tone frequency output， when TONE OFF the BZ pin output low level.
13-15	COM0-COM2	O	LCD COM outputs
16-28	SEG31,29,27,25,23,21,19,17,15,13,11,9,SEG7	O	LCD SEG outputs

4 Functional Description

4.1 Block diagram



4.2 Display RAM

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands.

The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0		
SEG0					0	address 6 bit （A5----A0）
SEG1					1	
SEG2					2	
SEG3					3	
⋮					⋮	
SEG31					31	
	D3	D2	D1	D0	Data\Addr	

4.3 System Oscillator

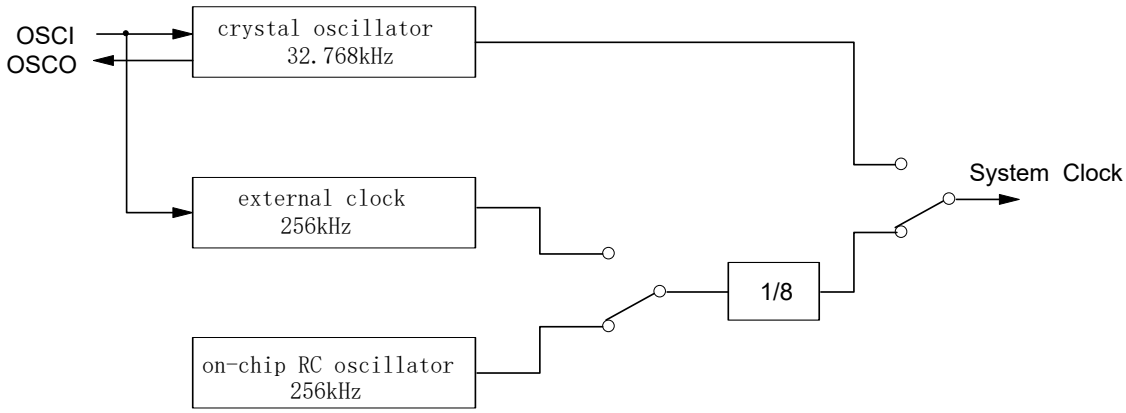
The VK1621 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. （e.g. 256khz clk generated by MCU pin）。

After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off,the LCD display will become blank, and the time base/WDT lose its function as well.That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the standby mode.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a standby command.

At the initial system power on, the VK1621 is at the SYS DIS state.

System Oscillator Configuration：



4.4 Time Base and WDT

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT) is composed of an 8-stage time base generator along with a 2-stage count-up counter,it is designed to break the host controller from abnormal states such as unknown or unwanted jump, execution errors, etc.The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the /IRQ pin by a command option. There are totally 8 frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

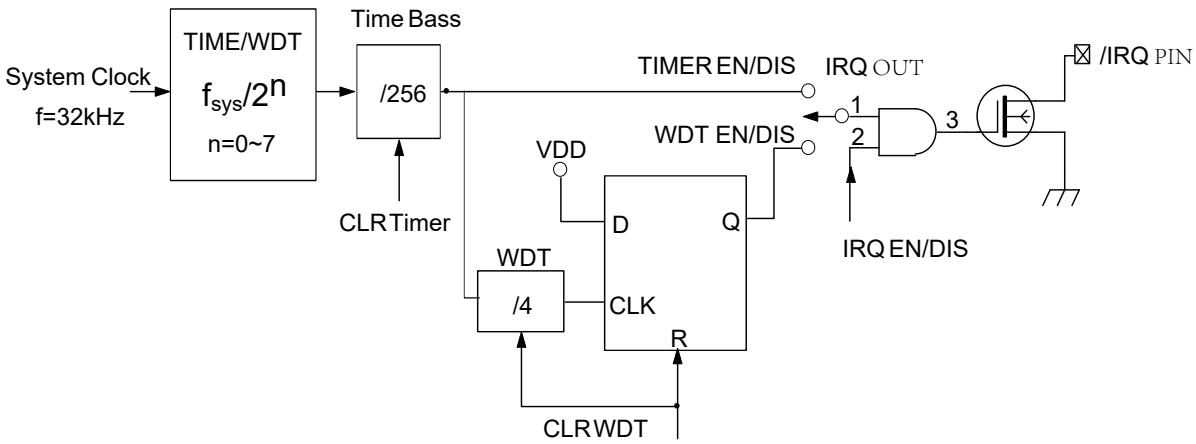
$f_{WDT}=f_{sys}/2^n$ （n=0~7） fsys=32kHz

The time base generator and WDT share the same 8-stage counter.WDT is cleared by executing the CLR WDT command,time base generator is cleared by executing the CLR WDT or the CLR TIMER command.

Executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the /IRQ pin). invoking the WDT DIS command disables the time base generator.After the TIMER EN command is transferred, the WDT is disconnected from the /IRQ pin, and the output of the time base generator is connected to the /IRQ pin.

The /IRQ output can be enabled or disabled by executing the IRQ EN or the IRQ DIS command. After the system power on, the /IRQ will be disabled.

Timer and WDT Configurations：



4.5 Tone Output

VK1621 has a simple 2KHz / 4kHz tone generator， it can output a pair of differential driving signals on the BZ and /BZ, which are used to generate a single tone By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and /BZ, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the /BZ outputs will remain at low level.

4.6 LCD Driver

The VK1621 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2COM or 3COM or 4COM by the software configuration.

4.6.1 Communication Interfacing

Four lines are required to interface with the VK1621.If only used for display, only 3 pins can be used.

The /CS pin is used to initialize the serial interface circuit and to terminate the communication with HOST.

. The DATA pin is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line.

The /RD line is the READ clock input. Data in the RAM are clocked out on the falling edge of the /RD signal, and the clocked out data will then appear on the DATA line

The /WR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into theVK1621 on the rising edge of the WR signal.

The /IRQ pin can be selected as a timer output or a WDT overflow flag output by the software setting,it is a NMOS open drain output..

4.6.2 Command Format

VK1621 can be configured by the Software setting.There are two mode commands to configure the LCD parameters and to transfer the LCD display data,The configuration mode of the VK1621 is called command mode, and its command mode ID is 1 0 0. The data mode includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode IDs and the command mode ID:

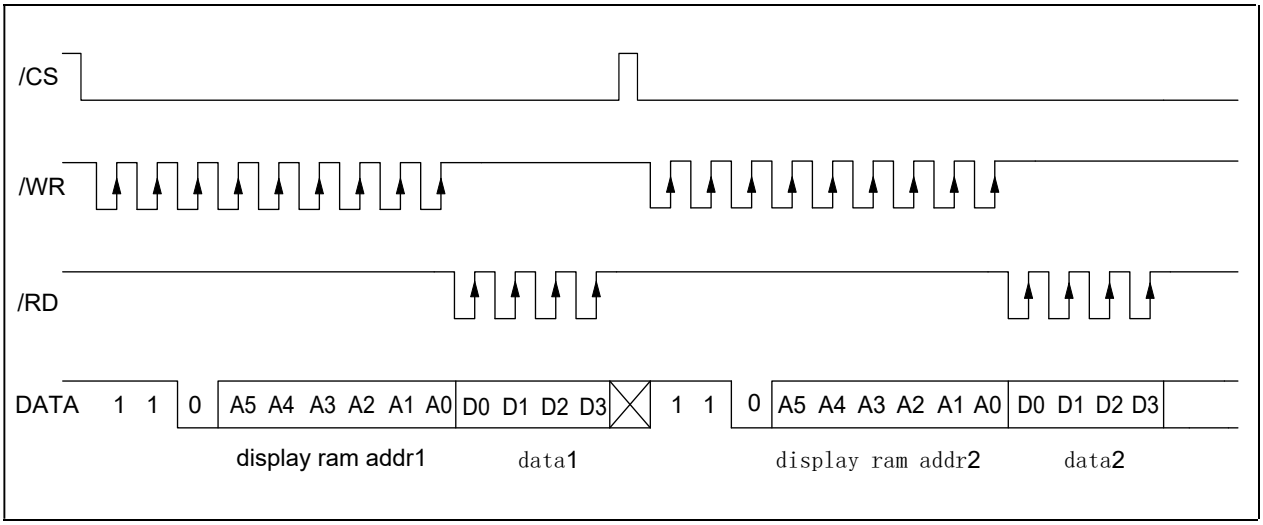
Operation	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

4.6.3 Cmd/Data Timing Diagrams

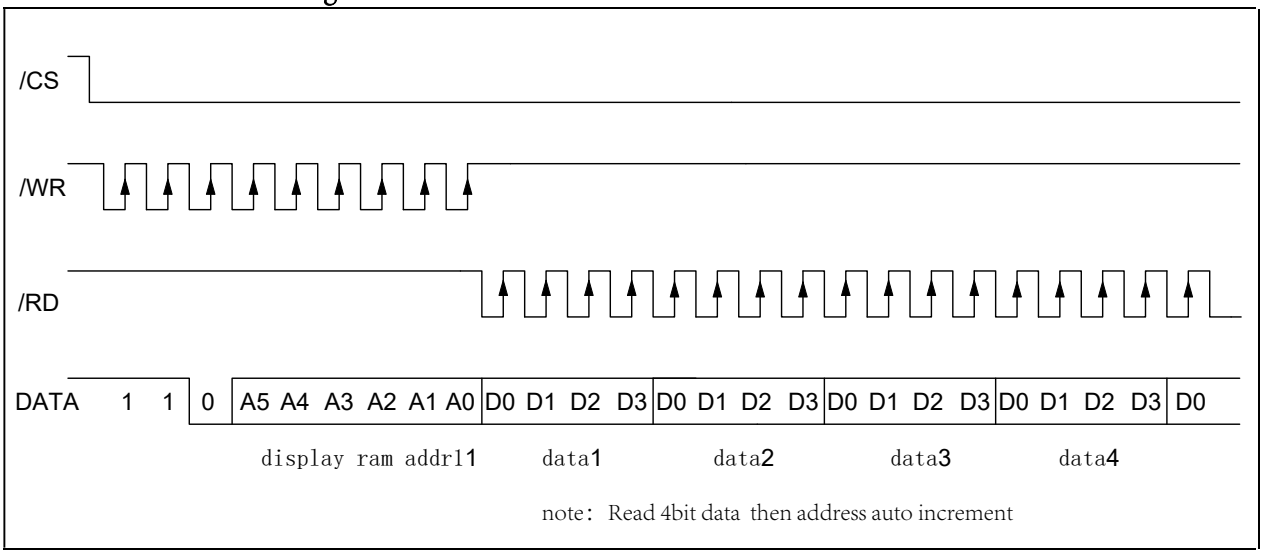
The following are the data mode IDs and the command mode ID Timing Diagrams。

4.6.3.1 READ Mode

Command Code : 110

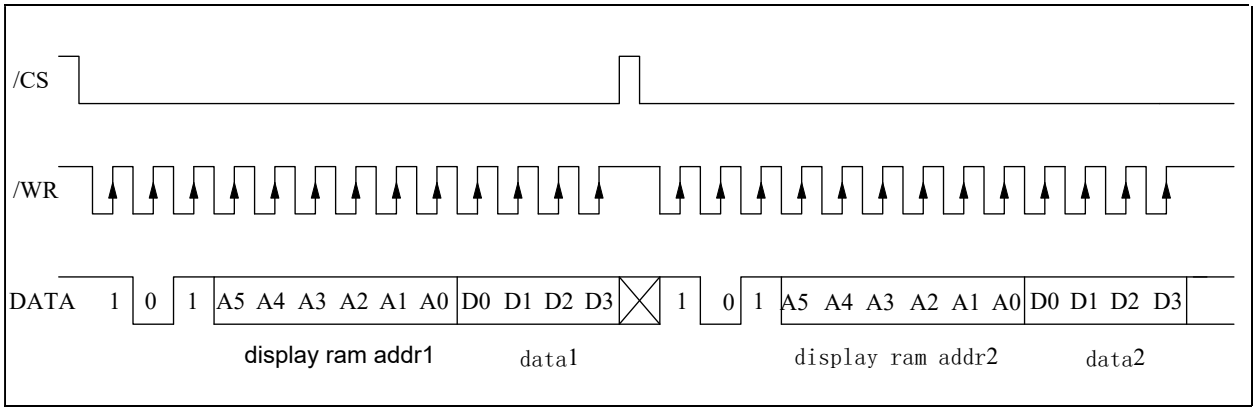


Successive Address Reading

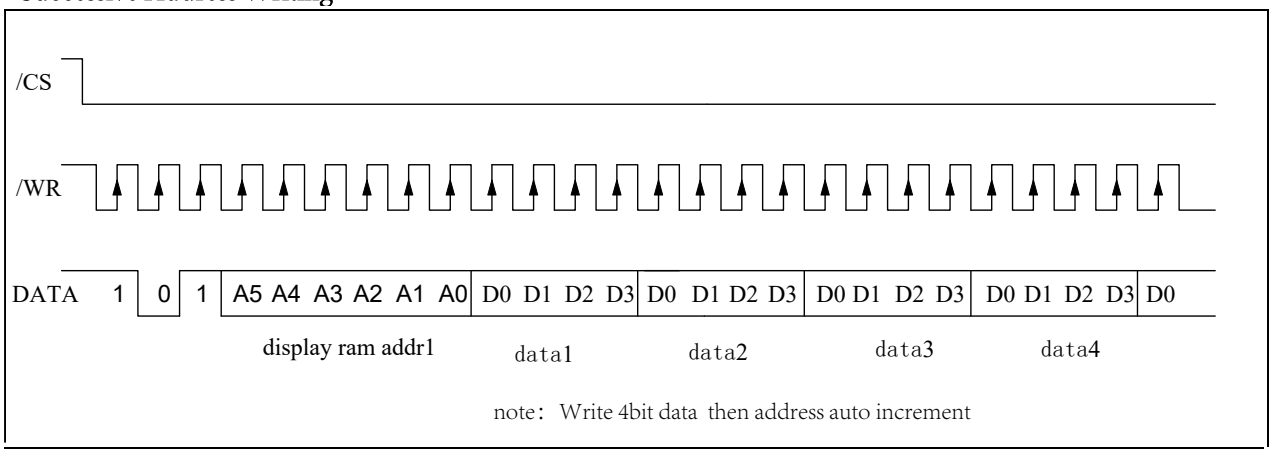


4.6.3.2 WRITE Mode

Command Code : 101

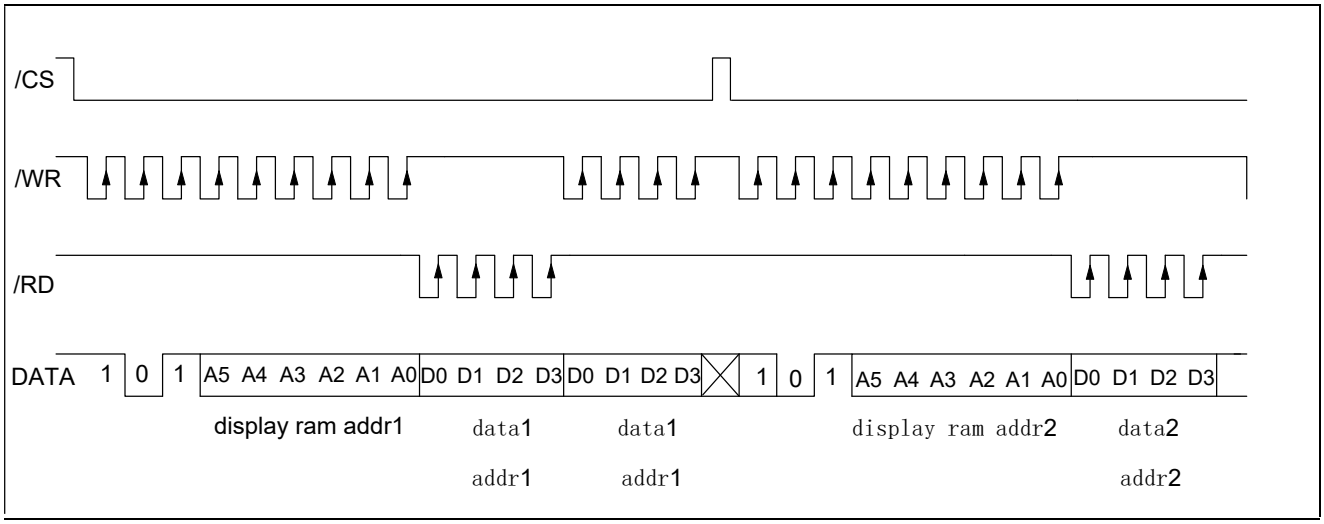


Successive Address Writing

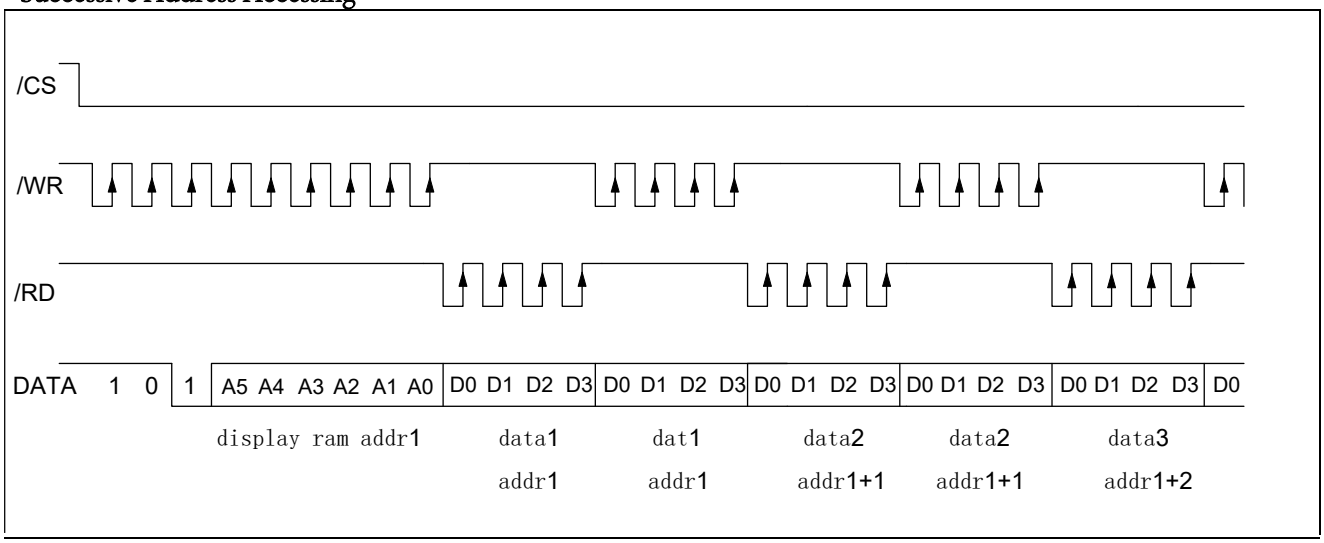


4.6.3.3 Read-Modify-Write Mode

Command Code : 101

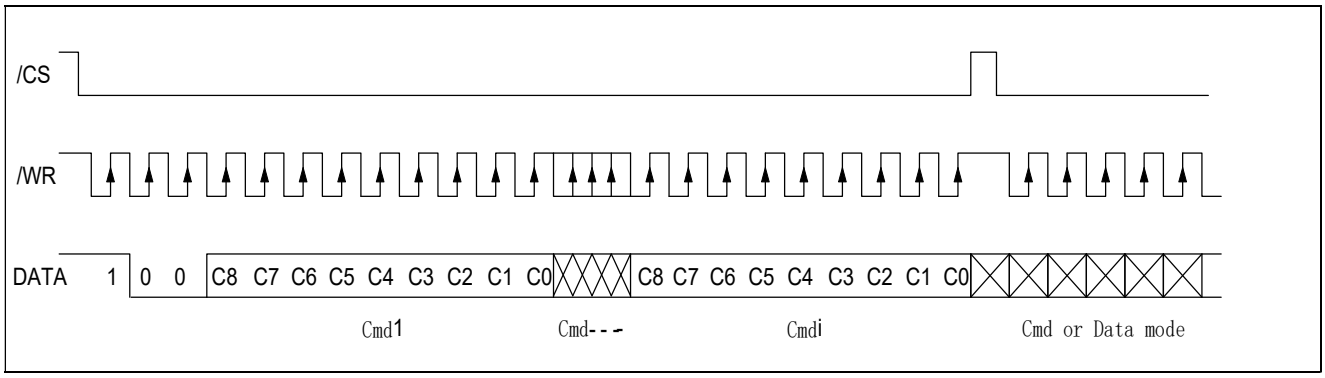


Successive Address Accessing



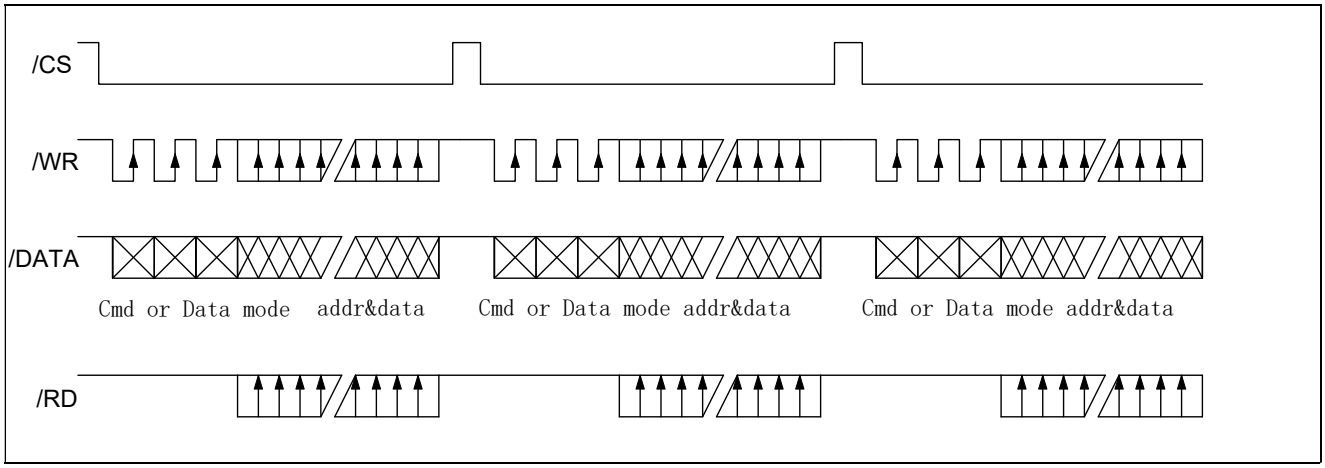
4.6.3.4 Command Mode

Command Code : 100



4.6.3.5 Data and Command Mode

Data and Command Mode



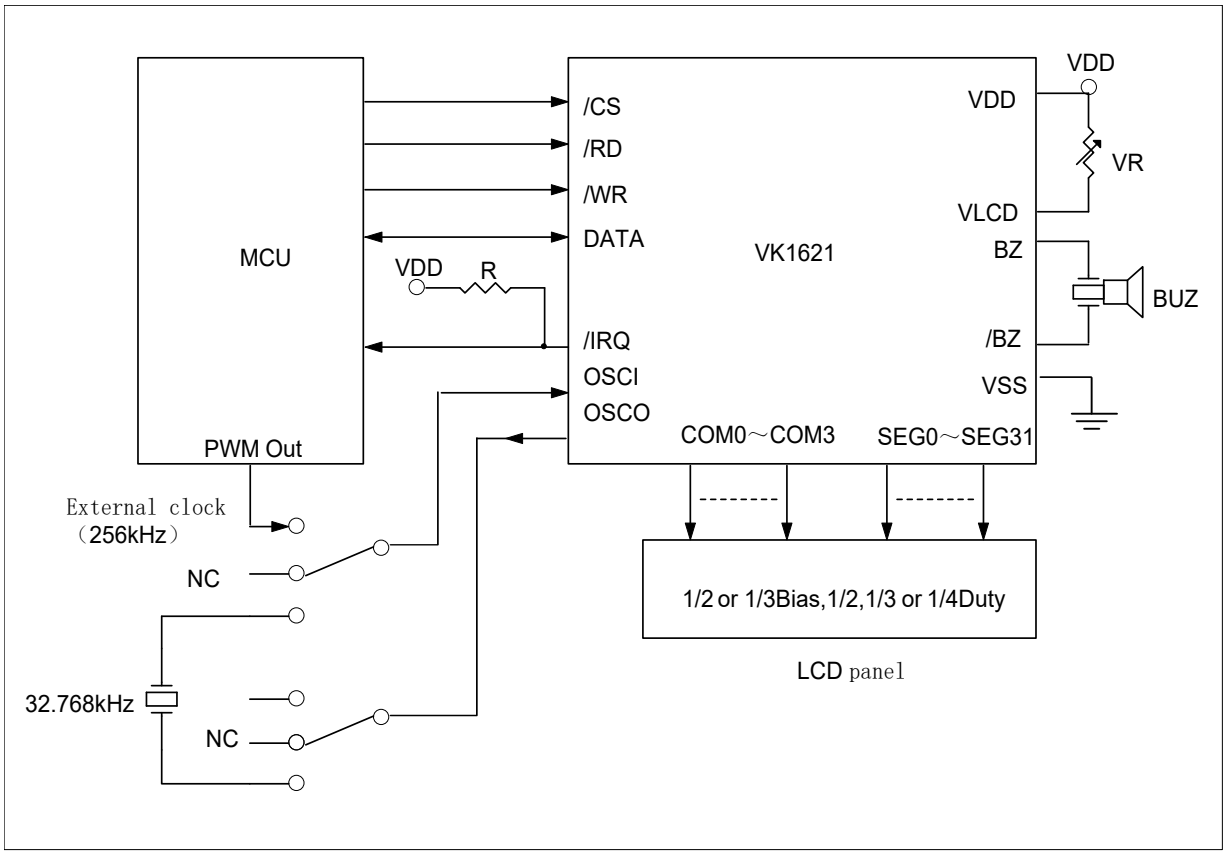
5 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000- 0000-X	C	Turn off system oscillator	YES
SYS EN	100	0000- 0001-X	C	Turn on system oscillator	
LCD OFF	100	0000- 0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000- 0011-X	C	Turn on LCD bias generator	
TIMERS DIS	100	0000- 0100-X	C	Disable time base output	
WDT DIS	100	0000- 0101-X	C	Disable WDT time-out flag outpu	
TIMER EN	100	0000- 0110-X	C	Enable time base output	
WDT EN	100	0000- 0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000- 1000-X	C	Turn off tone outputs	YES
TONE ON	100	0000- 1001-X	C	Turn on tone outputs	
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32k	100	0001-01XX-X	C	crystal oscillator	
RC 256k	100	0001-10XX-X	C	on-chip RC oscillator	YES
EXT 256k	100	0001-11XX-X	C	external clock source	
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2bias option ab=00：2 COMS ab=01：3 COMS ab=10：4 COMS	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 bias option ab=00：2 COMS ab=01：3 COMS ab=10：4 COMS	
TONE 4k	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2k	100	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	100	100X-0XXX-X	C	Disable IRQ output	YES
IRQ EN	100	100X-1XXX-X	C	Enable IRQ output	
F1	100	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110-0000- X	C	Test mode	
NORMAL	100	1110-0011- X	C	Normal mode	YES

Note：X：0 or 1
A5-A0: DIspaly RAM addresses
D3-D0:4bit DIspaly RAM data

D/C:Data/Command mode
Def.:Power on reset default
110,101 and 100 is Command ID

6 Application Circuits



Note：Adjust VR(20K) to fit user's LCD panel display voltage (VLCD)

7 Electrical characteristics

7.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～5.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	TSTG	-50～+125	℃
Operating Temperature	TOTG	-40～+85	℃

7.2 DC Characteristics

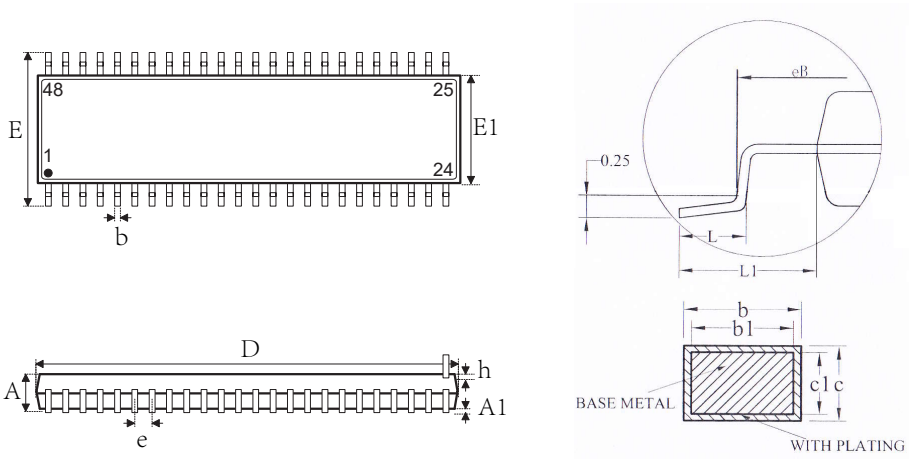
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I_{DD1}	—	150	300	μA	3V	No load/LCD ON On-chip RC oscillator
		—	300	600		5V	
Operating current	I_{DD2}	—	60	120	μA	3V	No load/LCD ON Crystal oscillator
		—	120	240		5V	
Operating current	I_{DD3}	—	100	200	μA	3V	No load/LCD ON External clock source
		—	200	400		5V	
Standby Current	I_{STB}	—	0.1	5	μA	3V	No load, Power down mode
		—	0.3	10		5V	
Input Low Voltage	V_{IL}	0	—	0.6	V	3V	DATA, /WR, /CS, /RD
		0	—	1.0		5V	
Input High Voltage	V_{IH}	2.4	—	3.0	V	3V	DATA, /WR, /CS, /RD
		4.0	—	5.0		5V	
DATA, BZ, /BZ, /IRQ	I_{OL1}	0.5	1.2	—	mA	3V	V_{OL}=0.3V
		1.3	2.6	—		5V	V_{OL}=0.5V
DATA, BZ, /BZ	I_{OH1}	-0.4	-0.8	—	mA	3V	V_{OH}=2.7V
		-0.9	-1.8	—		5V	V_{OH}=4.5V
LCD COM Sink Current	I_{OL2}	80	150	—	μA	3V	V_{OL}=0.3V
		150	250	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH2}	-80	-120	—	μA	3V	V_{OH}=2.7V
		-120	-200	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL3}	60	120	—	μA	3V	V_{OL}=0.3V
		120	200	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH3}	-40	-70	—	μA	3V	V_{OH}=2.7V
		-70	-100	—		5V	V_{OH}=4.5V
Pull-UP Resistor	R_{UP}	40	80	150	kΩ	3V	DATA, /WR, /CS, /RD
		30	60	100		5V	

7.3 AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	—	256	—	kHz	3V	On-chip RC oscillator
		—	256	—		5V	On-chip RC oscillator
System Clock	f_{SYS2}	—	32.768	—	kHz	3V	Crystal oscillator
		—	32.768	—		5V	
System Clock	f_{SYS3}	—	256	—	kHz	3V	External clock source
		—	256	—		5V	
LCD Clock	f_{LCD1}	—	f_{SYS1}/1024	—	Hz	—	On-chip RC oscillator
		—	f_{SYS2}/128	—			Crystal oscillator
		—	f_{SYS3}/1024	—			External clock source
LCD Common Period	t_{COM}	—	N/ f_{LCD}	—	sec	—	N： Number of COM
Serial Data Clock （/WR）	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Data Clock （/RD）	F_{CLK2}	—	—	75	kHz	3V	Duty cycle 50%
		—	—	150		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	μs	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	μs	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r, t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	

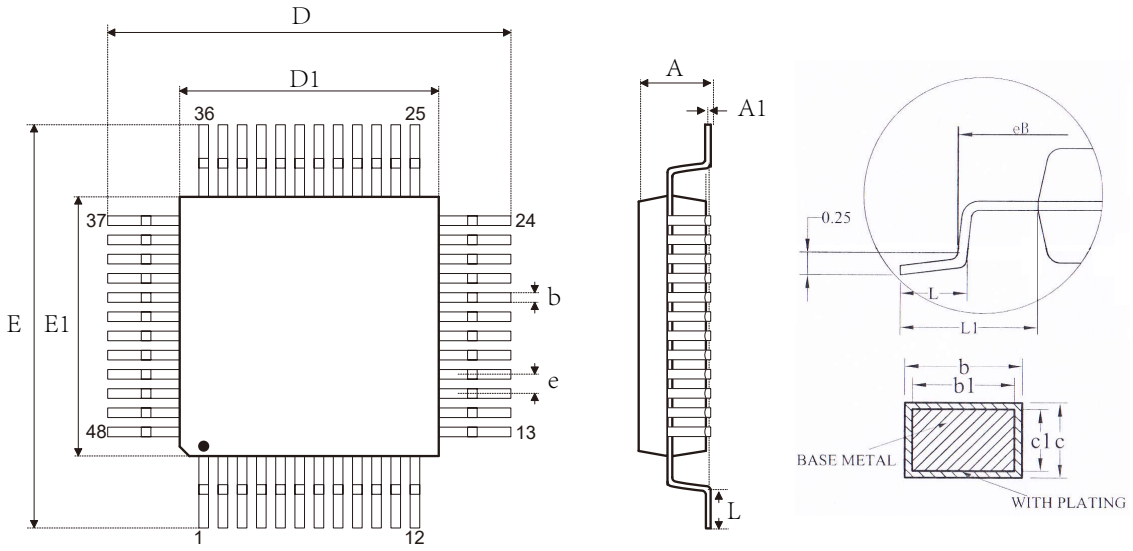
8 Package Information

8.1 SSOP48 (300mil) (15.9mm x 7.5mm PP=0.635mm)



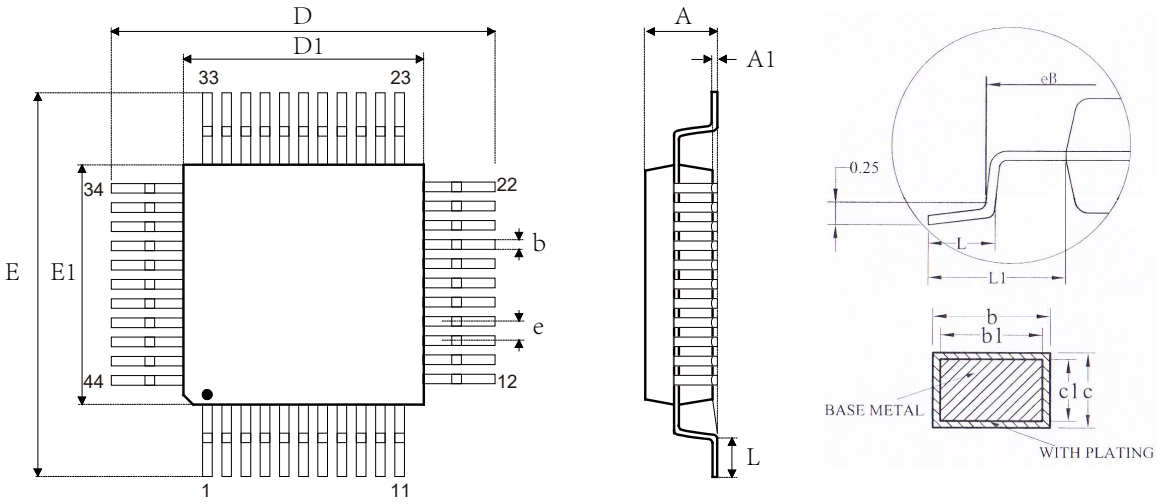
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	2.80
A1	0.20	0.30	0.40
b	0.24	--	0.33
b1	0.23	0.25	0.28
c	0.14	--	0.23
c1	0.13	0.15	0.18
D	15.80	15.90	16.00
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	0.635BSC		
h	0.30	--	0.50
L	0.61	--	0.91
L1	1.40REF		

8.2 LQFP48(7.0mm x 7.0mm PP=0.5mm):



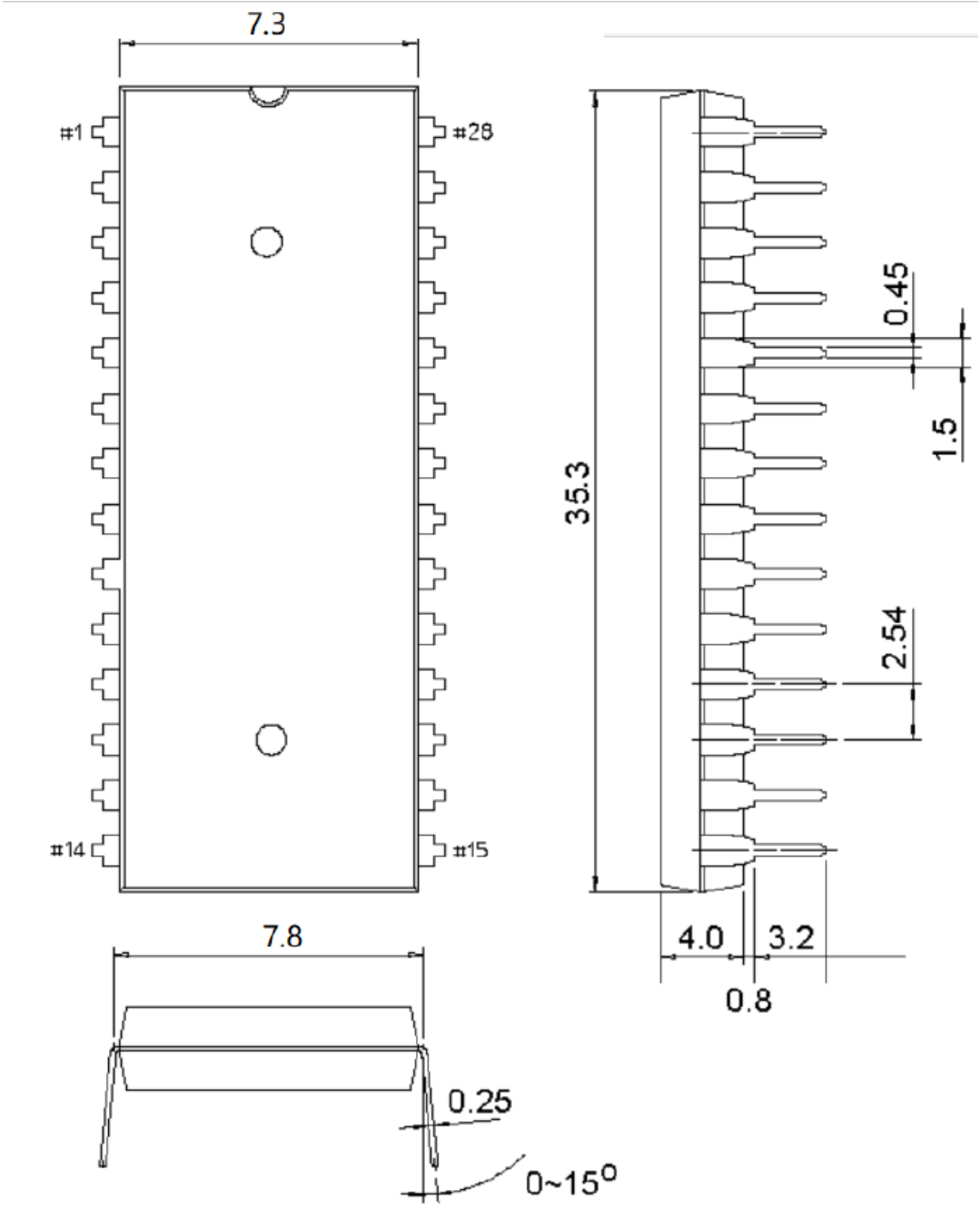
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		

8.3 LQFP44(10.0mm x 10.0mm PP=0.8mm):



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
b	0.28	--	0.36
b1	0.27	0.30	0.33
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80BSC		
L	0.45	--	0.75
L1	1.00REF		

8.3 SDIP28： (288mil)(35.3mm x 7.3mm PP=2.54mm)



9 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

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