

Features

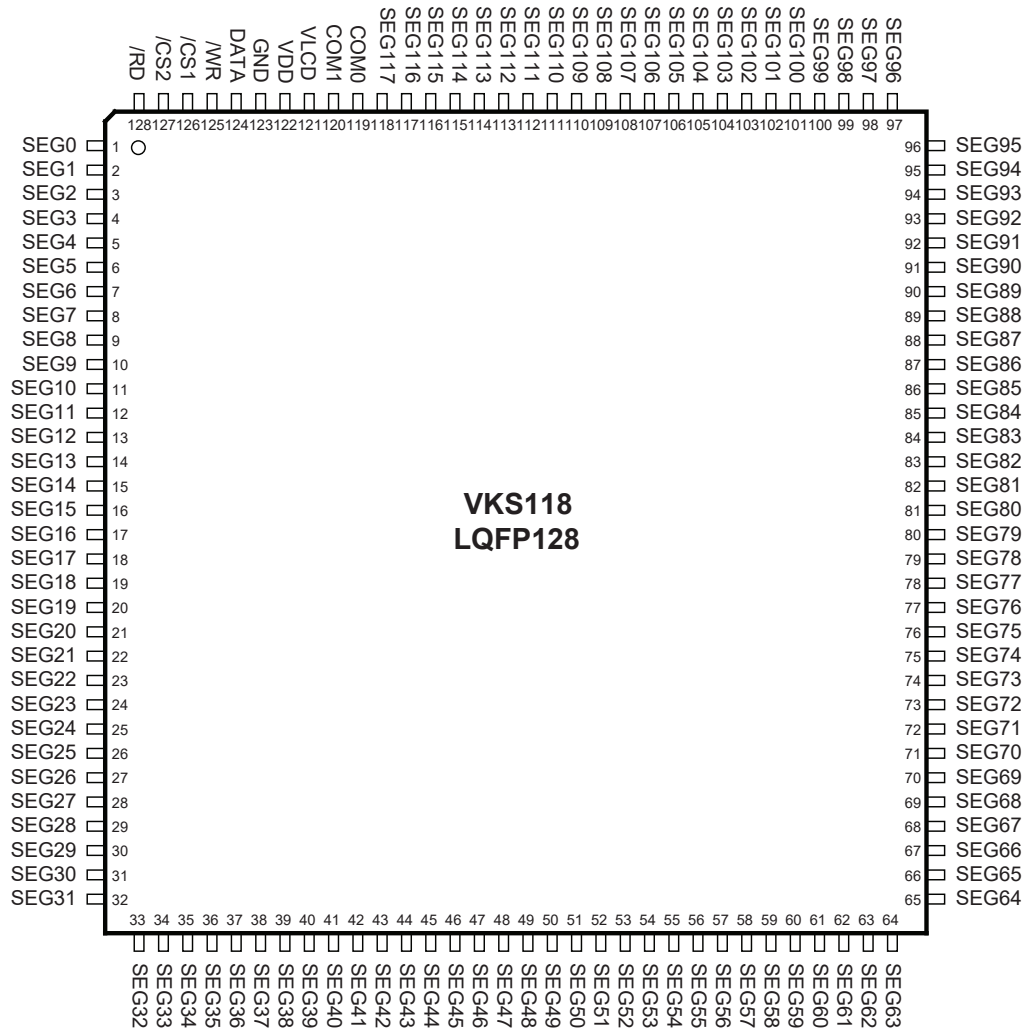
- Operating voltage: 2.4-5.2V
- Built-in 256kHz RC oscillator (default)
- static,no bias 100% duty
- Built-in display RAM
- STANDBY mode (by Cmd LCD OFF,SYS DIS) .
- 5 wire serial interface
- display mode 118×1
- Software configuration LCD parameters
- Data mode and command mode instructions
- Read/Write address auto increment
- VLCD pin for adjusting LCD operating voltage ($\leq VDD$)
- Three data accessing modes
- Package:
LQFP128(14.0mm x 14.0mm PP=0.4mm)

1 General Description

VKS118 is a RAM Mapping dual-mode LCD Driver. It can support static LCD screens with a maximum of 118 pattern(118SEGx1COM), 5 lines are required to communication interface with the VKS118,it is used to configure display parameters and transfer display data, and can also enter the standby mode through Power down command (by Cmd LCD OFF,SYS DIS) . It has the characteristics of good contrast, large viewing angle and no flicker. It is suitable for washing machine panels, automotive instruments, household appliances and other products requiring high display quality.

2 Pinouts and pin description

2.1 VKS118 LQFP128 Pin Assignment

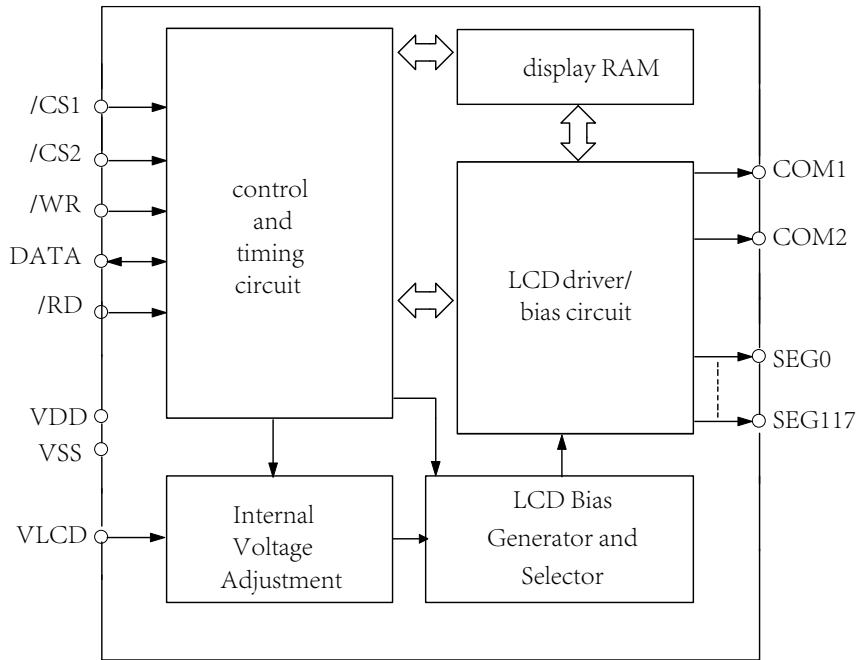


2.2 VKS118 LQFP128 Pin Description

No.	Name	I/O	Function
1-118	SEG0-SEG117	O	LCD SEG outputs
119-120	COM0,COM1	O	LCD COM outputs
121	VLCD	I	LCD power input
122	VDD	VDD	Positive power supply
123	VSS	VSS	Negative power supply
124	DATA	I/O	Serial data input/output with pull-high resistor.
125	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
126	/CS1	I	Page selection 1
127	/CS2	I	Page selection 2
128	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.

3 Functional Description

3.1 Block diagram



3.2 Display RAM

The display memory (RAM) is organized into 59×2 bit stores the displayed data. the contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the WRITE commands. The built-in RAM is divided into two pages, and the corresponding enable terminals are /CS1 and /CS2 pin. The first page is 32×2 Bit corresponding to SEG0-SEG63, and the second page is 27×2 Bit corresponding to SEG64-SEG117.

The following is a mapping from the RAM to the LCD pattern:

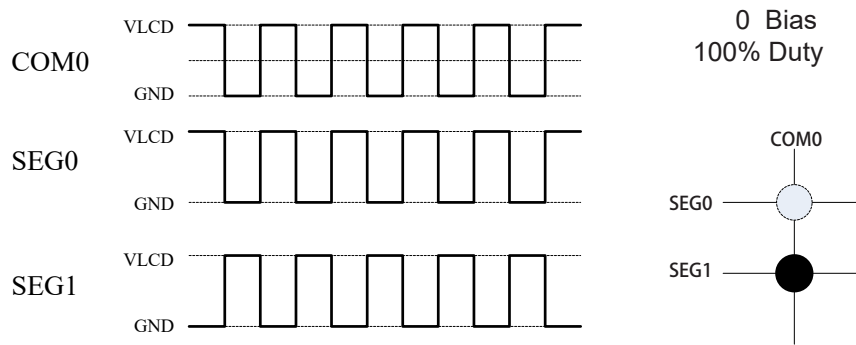
Two-way static (COM0.COM1 signals are the same) :

		COM0			
		SEG0	SEG1	0	first page address 6 bit (A5,A4--A0) /CS1 enable
		SEG2	SEG3	1	
		SEG4	SEG5	2	
		SEG6	SEG7	3	
		⋮	⋮		
		SEG62	SEG63	31	
D3	D2	D1	D0	Data/Addr	
		SEG64	SEG65	0	first page address 6 bit (A5,A4--A0) /CS2 enable
		SEG66	SEG67	1	
		SEG68	SEG69	2	
		SEG70	SEG71	3	
		⋮	⋮		
		SEG116	SEG117	26	
D3	D2	D1	D0	Data/Addr	

3.3 LCD Driver

VKS118 is a RAM Mapping dual-mode LCD Driver, drive display points 118×1, static display, no bias 100% duty. Built-in RC oscillator.

LCD driving waveform is as follows:



Note: To increase the drive capability of COM0, COM0, COM1 signals are the same.

3.3.1 Communication Interfacing

FIVE lines are required to interface with the VKS232.

\overline{CSn} pin is used to initialize the serial interface circuit and to terminate the communication with HOST. \overline{CSn} low level enables, The precautions for using the 2 chip selection feet are as follows:

- I. Only $\overline{CS1}$ is valid in command mode.
- II. Both write modes $\overline{CS1}$ and $\overline{CS2}$ are valid (When $\overline{CS1}$ and $\overline{CS2}$ are low at the same time, data will be written to 2 pages of RAM at the same time. Avoid this)
- III. Read mode does not allow the situation where $\overline{CS1}$ and $\overline{CS2}$ are low at the same time, otherwise it will cause status conflicts and display errors.

The DATA pin is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line.

The \overline{RD} line is the READ clock input. Data in the RAM are clocked out on the falling edge of the \overline{RD} signal, and the clocked out data will then appear on the DATA line

The \overline{WR} line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the VKS118 on the rising edge of the WR signal.

3.3.2 Command Format

VKS118 can be configured by the Software setting. There are two mode commands to configure the LCD parameters and to transfer the LCD display data, The configuration mode of the VKS118 is called command mode, and its command mode ID is 1 0 0. The data mode includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode IDs and the command mode ID:

Operation	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

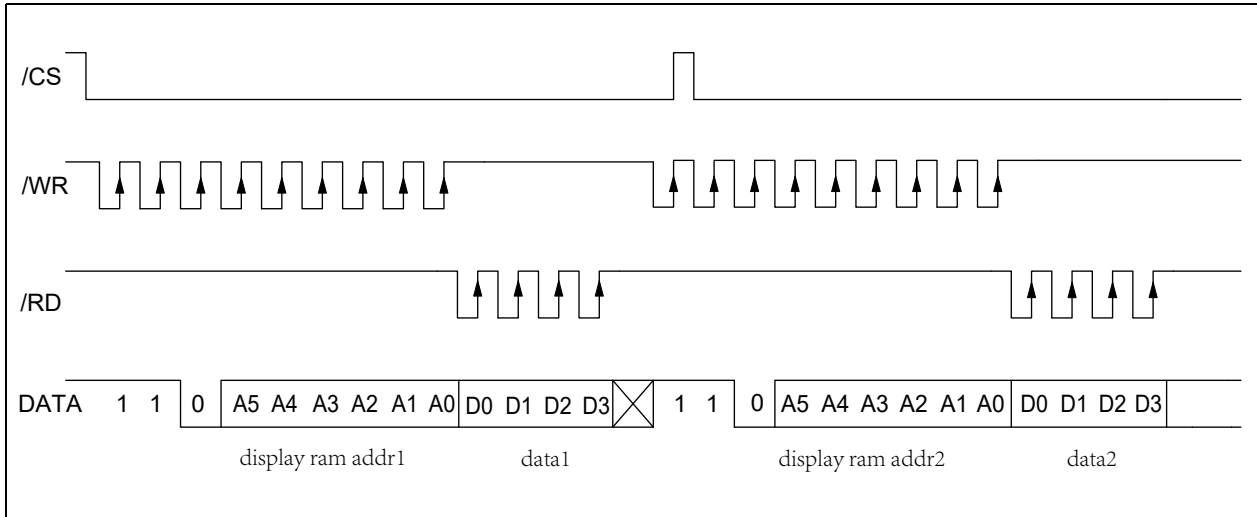
Note:

When the command mode /CS1 and /CS2 are at low level at the same time, the command is only valid for /CS1. In write mode, when /CS1 and /CS2 are at low level at the same time, they are valid at the same time. Read mode does not allow the situation where /CS1 and /CS2 are low at the same time, otherwise it will cause status conflicts and display errors.

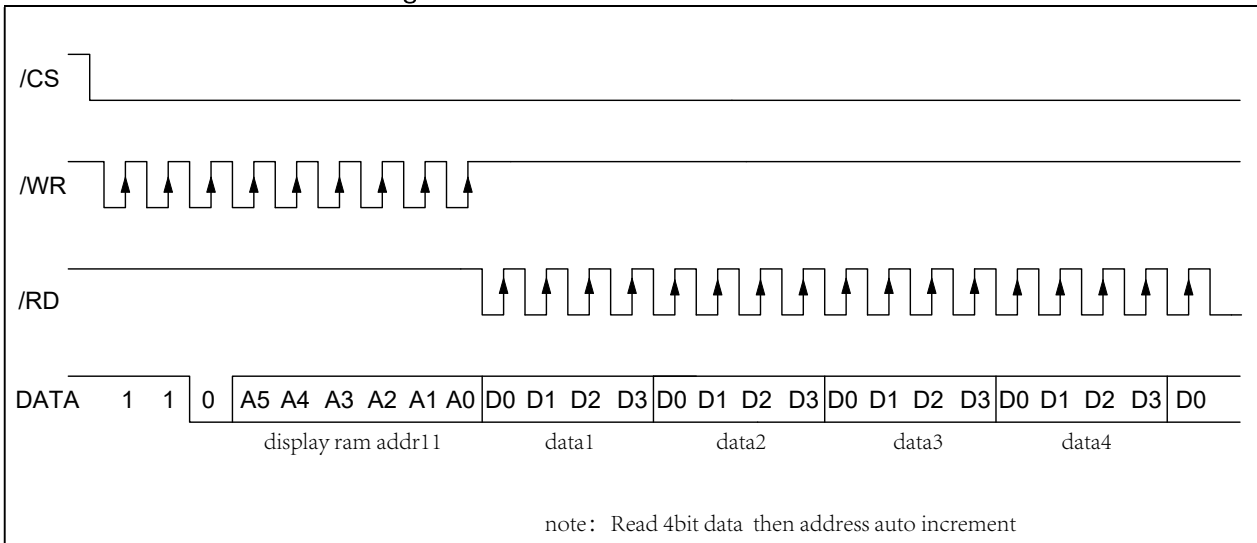
3.3.3 Cmd/Data Timing Diagrams

3.3.3.1 READ Mode

Command Code : 110

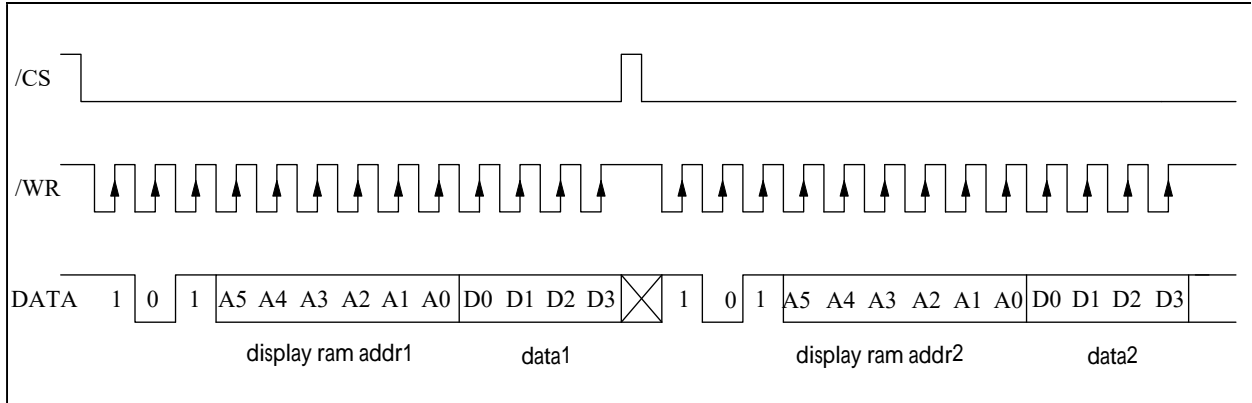


Successive Address Reading

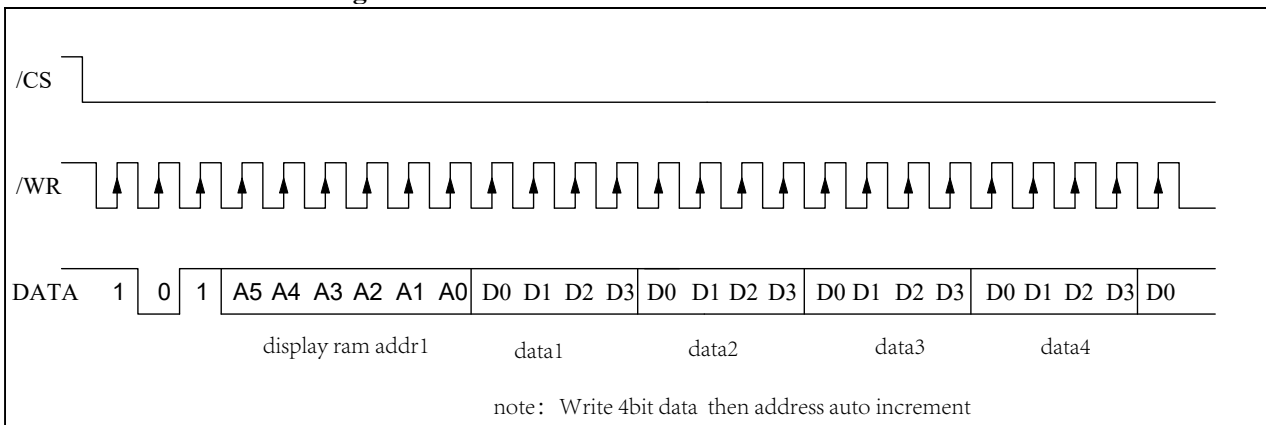


3.3.3.2 WRITE Mode

Command Code : 101

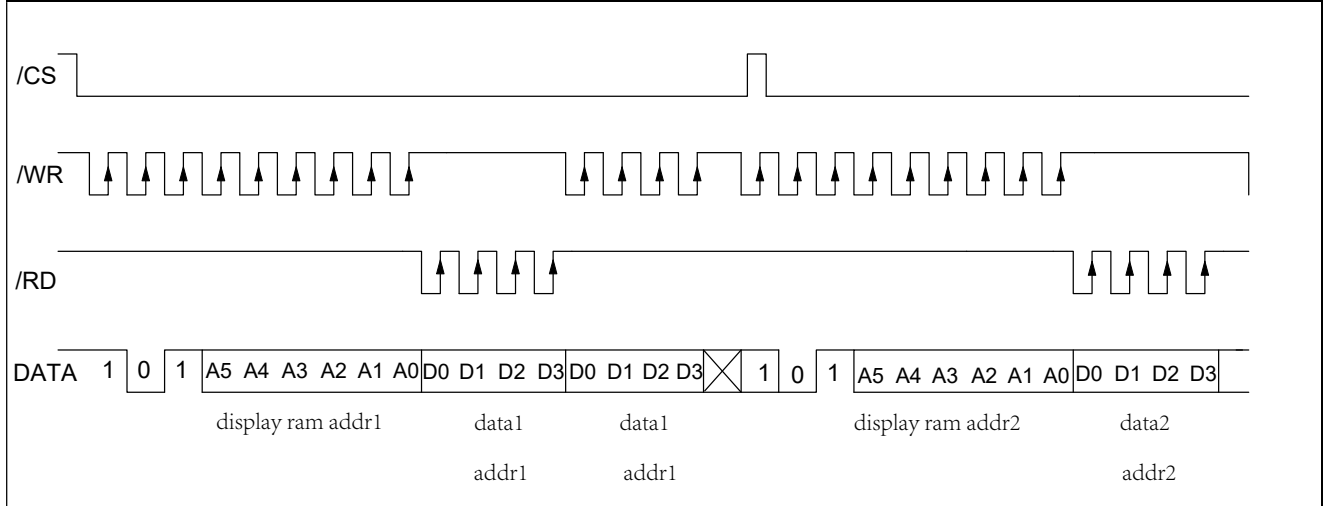


Successive Address Writing

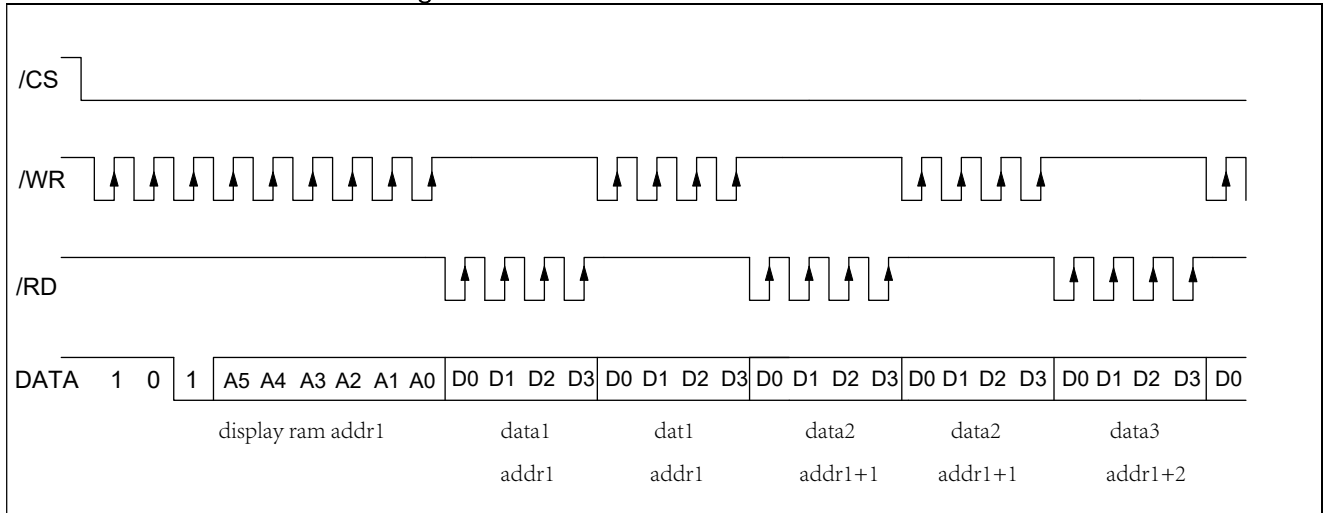


3.3.3.3 Read-Modify-Write Mode

Command Code : 101

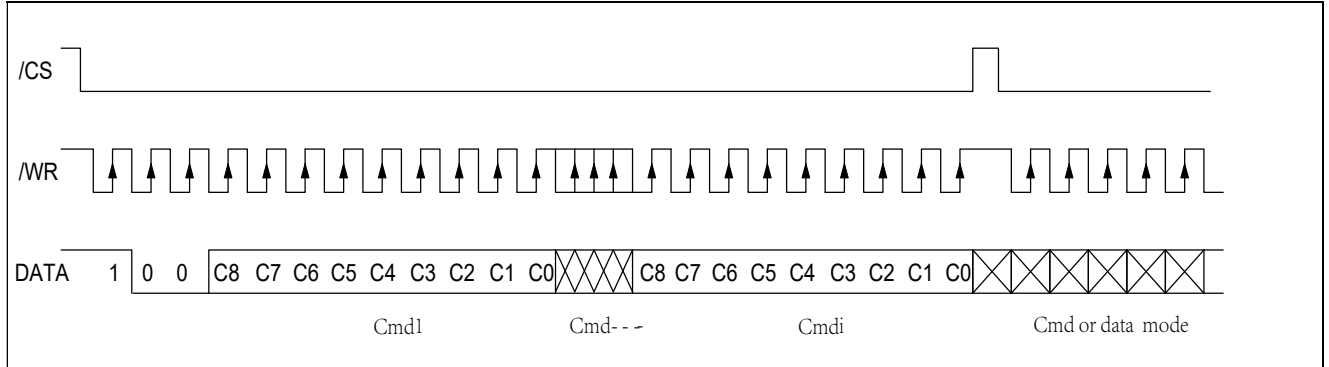


Successive Address Accessing



3.3.3.4 Command Mode

Command Code : 100



4 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000- 0000-X	C	Turn off both system oscillator	YES
SYS EN	100	0000- 0001-X	C	Turn on system oscillator	
LCD OFF	100	0000- 0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000- 0011-X	C	Turn on LCD bias generator	

note: X: 0 or 1

A5-A0: Display RAM addresses

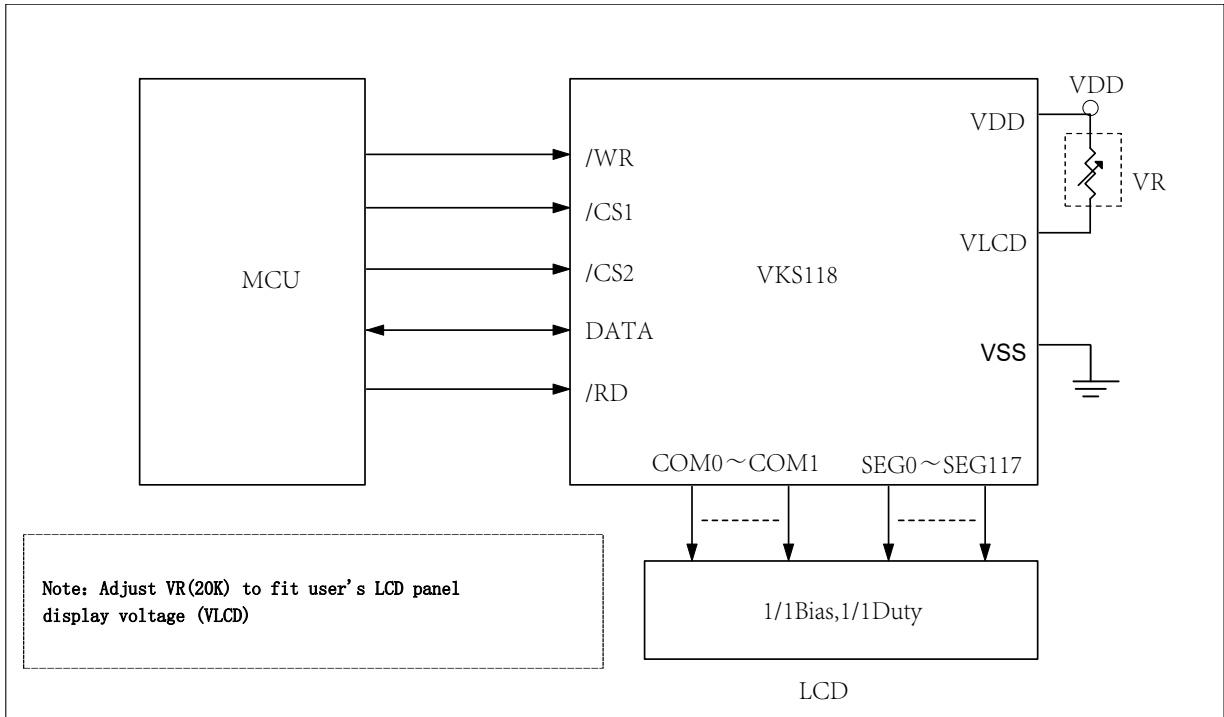
D3-D0: 4bit Display RAM data

D/C: Data/Command

mode Def.: Power on reset default

110, 101 and 100 is Command ID

5 Application Circuits



6 Electrical characteristics

6.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3 ~ 5.5	V
Input Voltage	VIN	V _{SS} -0.3 ~ V _{DD} +0.3	V
Storage Temperature	TSTG	-50 ~ +125	°C
Operating Temperature	TOTG	-40 ~ +85	°C

6.2 DC Characteristics

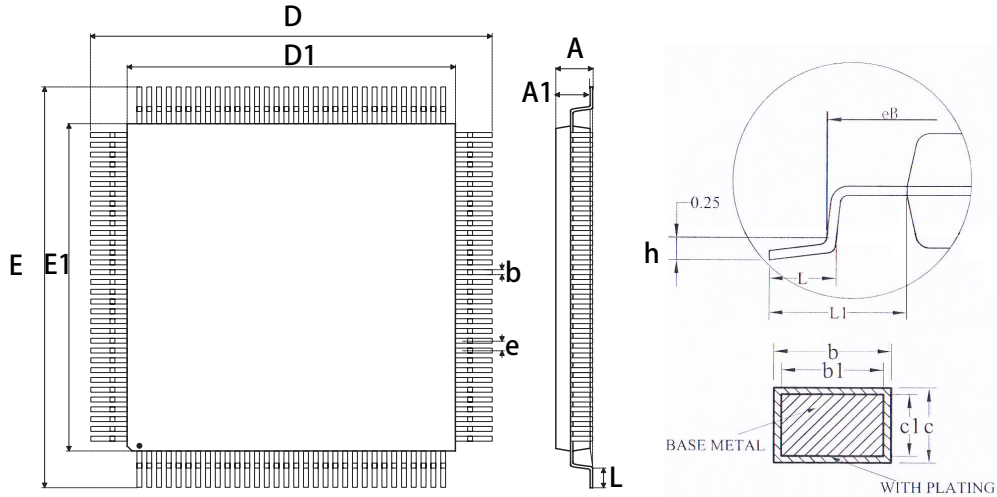
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I _{DD1}	—	150	300	μA	3V	No load/LCD ON
		—	300	600		5V	On-chip RC oscillator
Standby Current	I _{STB}	—	0.1	5	μA	3V	No load, Power down mode
		—	0.3	10		5V	
Input Low Voltage	V _{IL}	0	—	0.6	V	3V	DATA,/WR,/CS
		0	—	1.0		5V	
Input High Voltage	V _{IH}	2.4	—	3.0	V	3V	DATA,/WR,/CS
		4.0	—	5.0		5V	
DATA	I _{OL}	0.5	1.2	—	mA	3V	VOL=0.3V
		1.3	2.6	—		5V	VOL=0.5V
DATA	I _{OH}	-0.4	-0.8	—	mA	3V	VOL=2.7V
		-0.9	-1.8	—		5V	VOL=4.5V
LCD COM Sink Current	I _{OL1}	80	150	—	μA	3V	VOL=0.3V
		150	250	—		5V	VOL=0.5V
LCD COM Source Current	I _{OH1}	-80	-120	—	μA	3V	VOH=2.7V
		-120	-200	—		5V	VOH=4.5V
LCD SEG Sink Current	I _{OL2}	60	120	—	μA	3V	VOL=0.3V
		120	200	—		5V	VOL=0.5V
LCD SEG Source Current	I _{OH2}	-40	-70	—	μA	3V	VOH=2.7V
		-70	-100	—		5V	VOH=4.5V
Pull-UP Resistor	R _{PH}	40	80	150	KΩ	3V	DATA,/WR,/CS
		30	60	100		5V	

6.3 AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	192	256	320	kHz	3V	On-chip RC oscillator
		—	256	—		5V	
LCD Clock	f_{LCD1}	—	$f_{SYS1}/1024$	—	Hz	—	On-chip RC oscillator
LCD Common Period	t_{COM}	—	N/f_{LCD}	—	sec	—	N: Number of COM
Serial Data Clock (/WR,/RD)	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS1,/CS2
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	μ s	3V	Write mode
		1.67	—	—	μ s	5V	Write mode
Rise/Fall Time Serial Data Clock Width	t_r, t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	

7 Package Information

7.1 LQFP128(14.0mm x 14.0mm PP=0.4mm))



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	1.35	1.40	1.45
b	0.14	--	0.23
b1	0.13	0.16	0.19
c	0.13	--	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	15.20
E1	13.90	14.00	14.10
e	0.. 0BSC		
L	0.45	0.60	0.75
L1	1.00REF		

8 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

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